

FIG.1

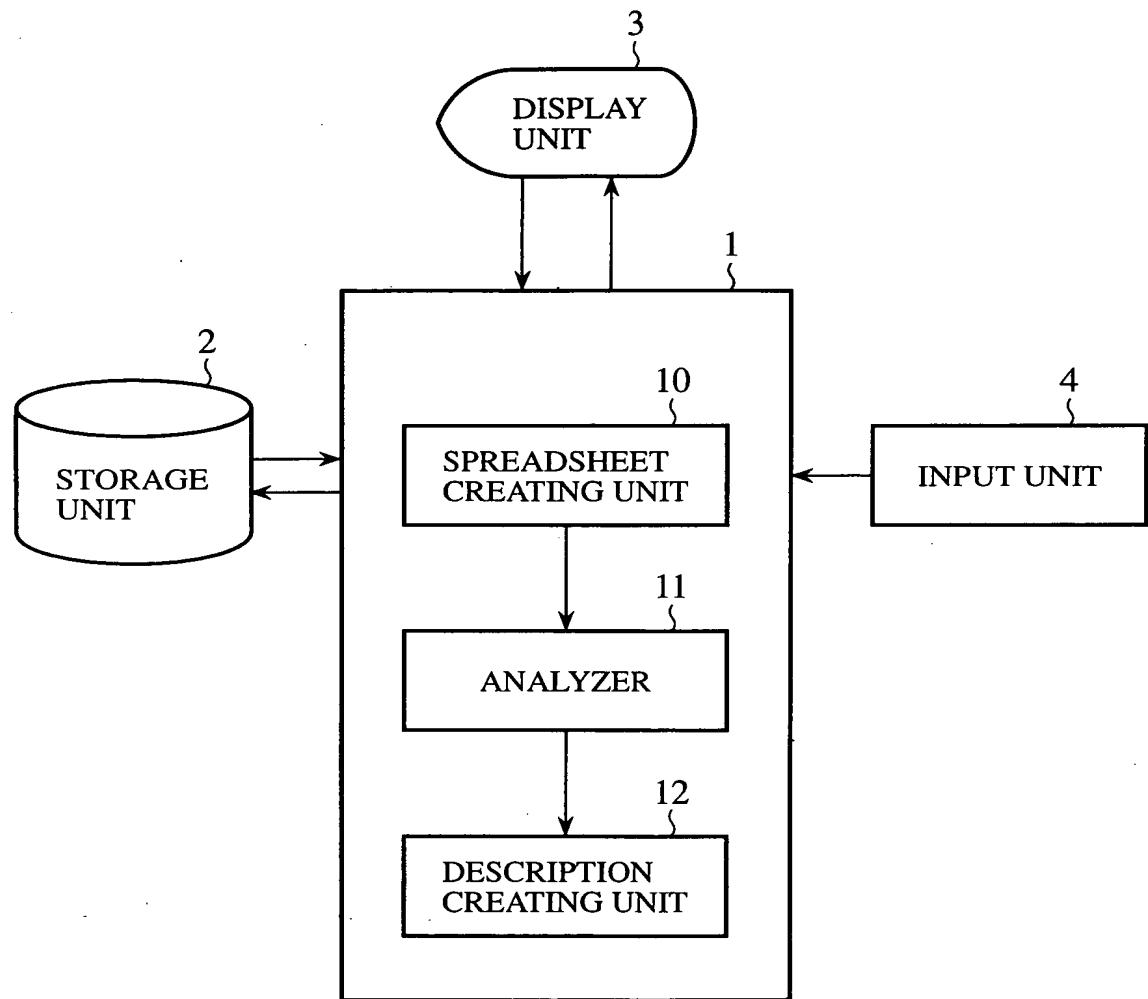


FIG.2

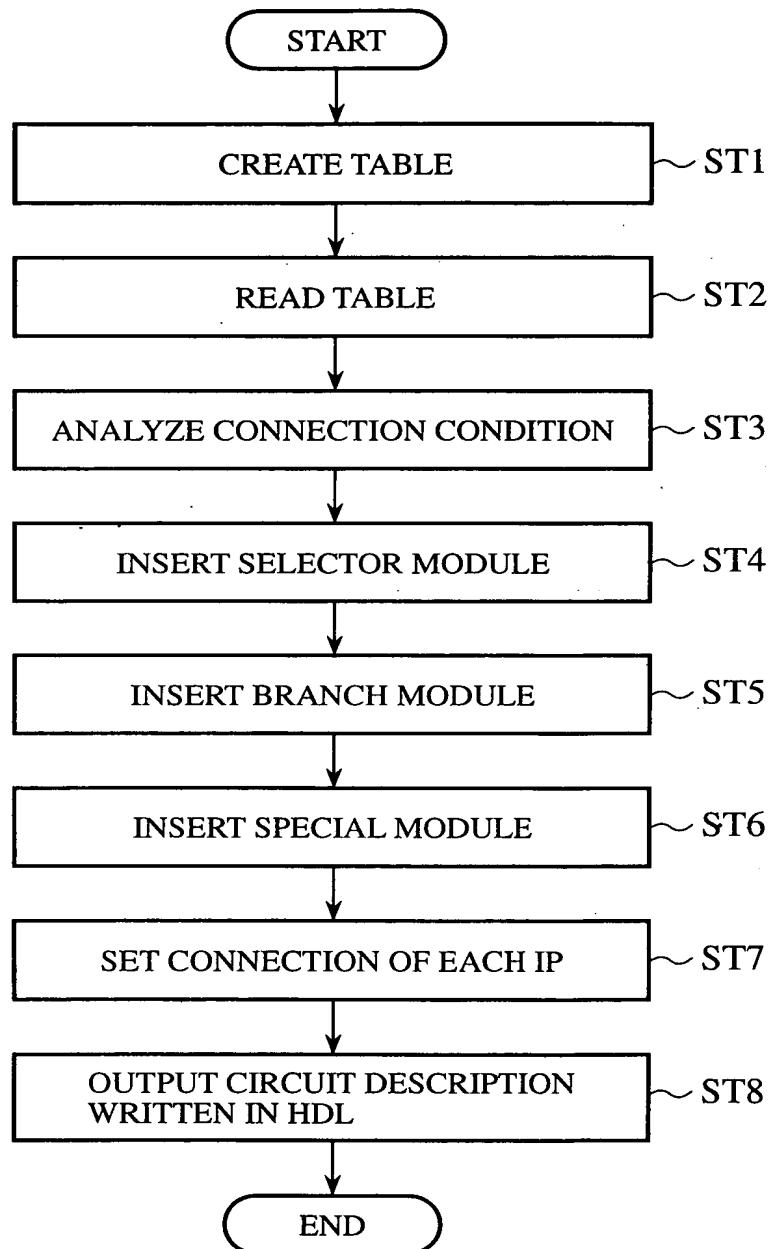


FIG.3

| PIN NAME | CONNECTION CONDITION 1 | CONNECTION CONDITION 2 | CONNECTION CONDITION 3 |
|----------|------------------------|------------------------|------------------------|
| PA       | IPA1                   | IPB1                   | IPC1                   |
| PB       | IPA2                   | IPA2                   | IPA2                   |
| PC       | IPA3                   | IPB2                   | IPC2                   |
| PD       | IPA4                   | IPA4                   | IPC3                   |

FIG.4

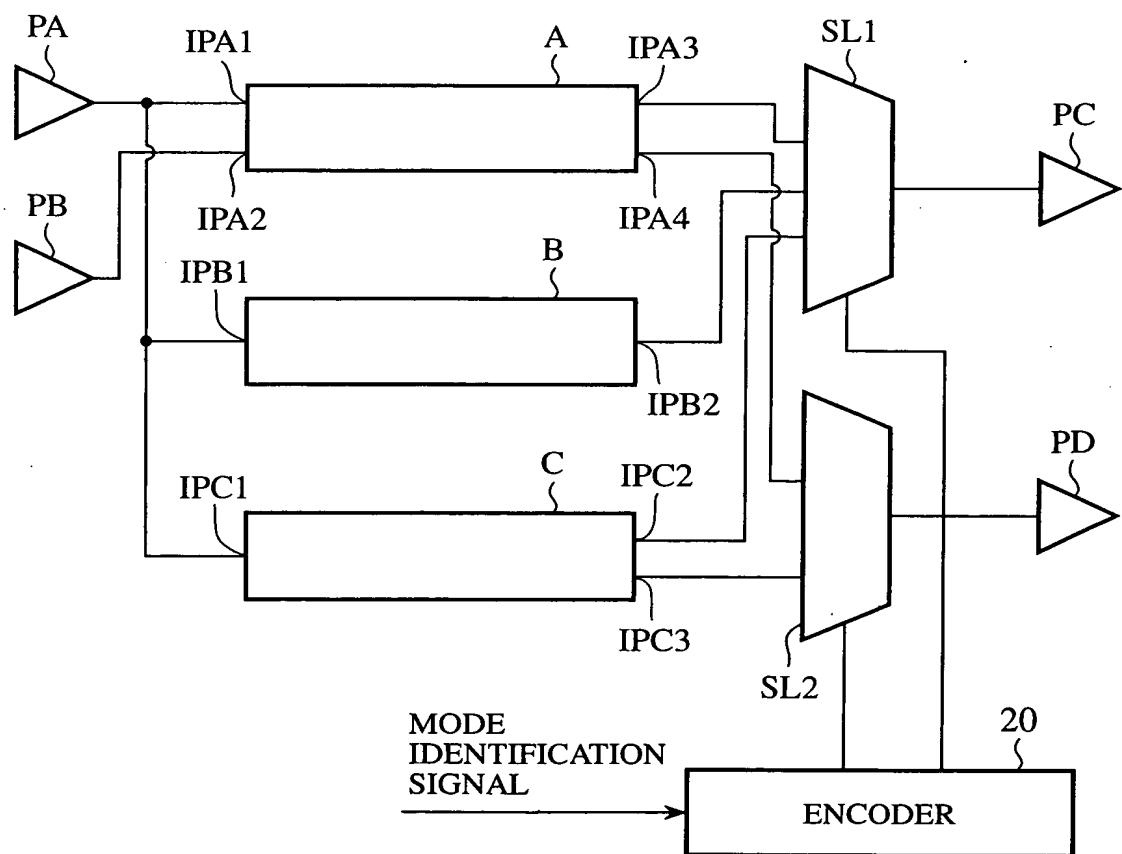


FIG.5

```
module TOP (PA, PB, PC, PD);  
    input PA, PB;  
    output PC, PD;  
    if (CONNECTION CONDITION 1 == 1'b1) begin  
        assign PA: = IPA1;
```

FIG.6

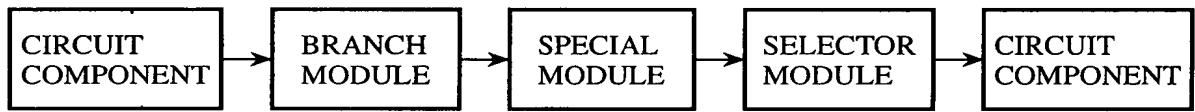


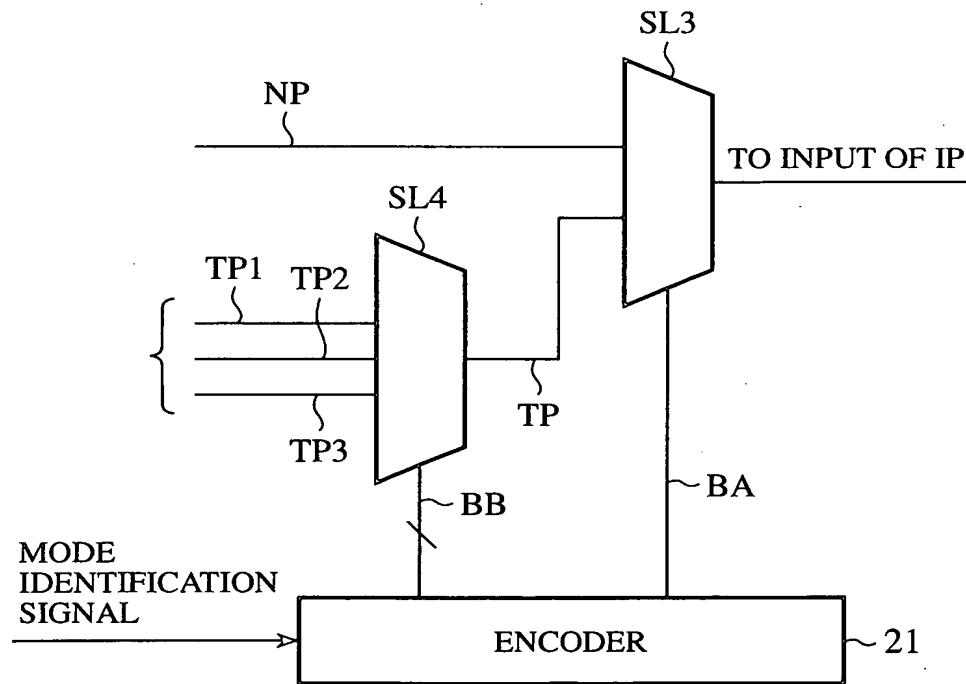
FIG.7

```
if (CONDITION LOGICAL EXPRESSION 1)  
    MODE IDENTIFICATION SIGNAL 1 = ACTIVE  
else  
    MODE IDENTIFICATION SIGNAL 1 = INACTIVE  
end  
if (CONDITION LOGICAL EXPRESSION 2)  
    MODE IDENTIFICATION SIGNAL 2 = ACTIVE  
else  
    MODE IDENTIFICATION SIGNAL 2 = INACTIVE  
end
```

FIG.8

| PIN NAME | NORMAL USE MODE | TEST MODE 1 | TEST MODE 2 | TEST MODE 3 |
|----------|-----------------|-------------|-------------|-------------|
|          |                 |             |             |             |
|          |                 |             |             |             |
|          |                 |             |             |             |
|          |                 |             |             |             |
|          |                 |             |             |             |
|          |                 |             |             |             |

FIG.9



## FIG.10

```
if (BA == 1)
    INPUT OF IP = NP
else
    INPUT OF IP = OUTPUT OF SELECTOR MODULE SL4
end
if (BB == 1)
    OUTPUT OF SELECTOR MODULE SL4 = TEST PATH TP1
else if (BB == 2)
    OUTPUT OF SELECTOR MODULE SL4 = TEST PATH TP2
else
    OUTPUT OF SELECTOR MODULE SL4 = TEST PATH TP3
end.
```

## FIG.11

```
if (MODE IDENTIFICATION SIGNAL 1 == 1)
    BA = SELECTION OF NORMAL PATH
    BB = SELECTION OF TEST PATH TP1
else if (MODE IDENTIFICATION SIGNAL 2 == 1)
    BA = SELECTION OF TEST PATH
    BB = SELECTION OF TEST PATH TP1
else if (MODE IDENTIFICATION SIGNAL 3 == 1)
    BA = SELECTION OF TEST PATH
    BB = SELECTION OF TEST PATH TP2
else
    BA = SELECTION OF TEST PATH
    BB = SELECTION OF TEST PATH TP3
end
```

Title: AUTOMATIC CIRCUIT DESIGN APPARATUS AND COMPUTER-IMPLEMENTED AUTOMATIC CIRCUIT  
DESIGN METHOD  
Inventors: NAGASAWA et al.  
Atty Docket No.: 402924  
Leydig, Voit & Mayer 202-737-6770  
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FIG.12

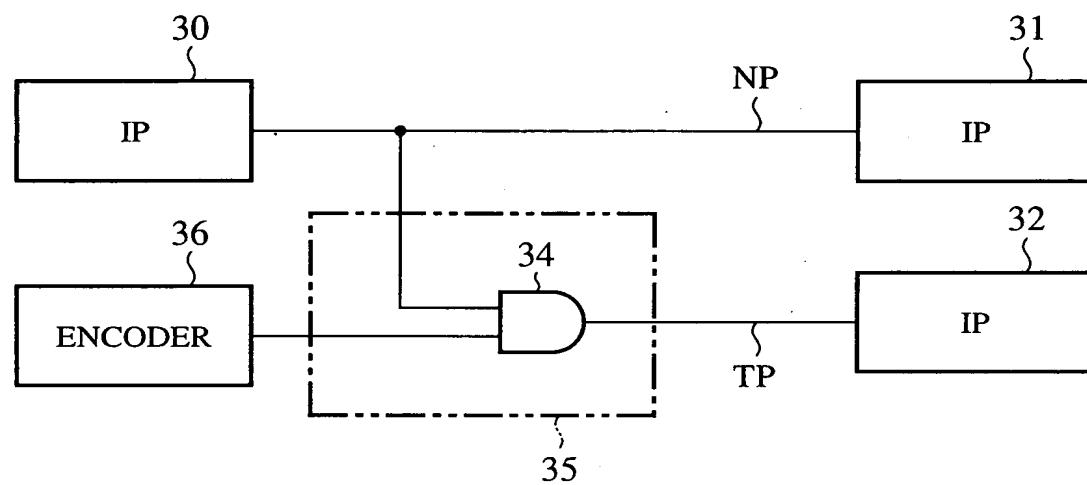


FIG.13

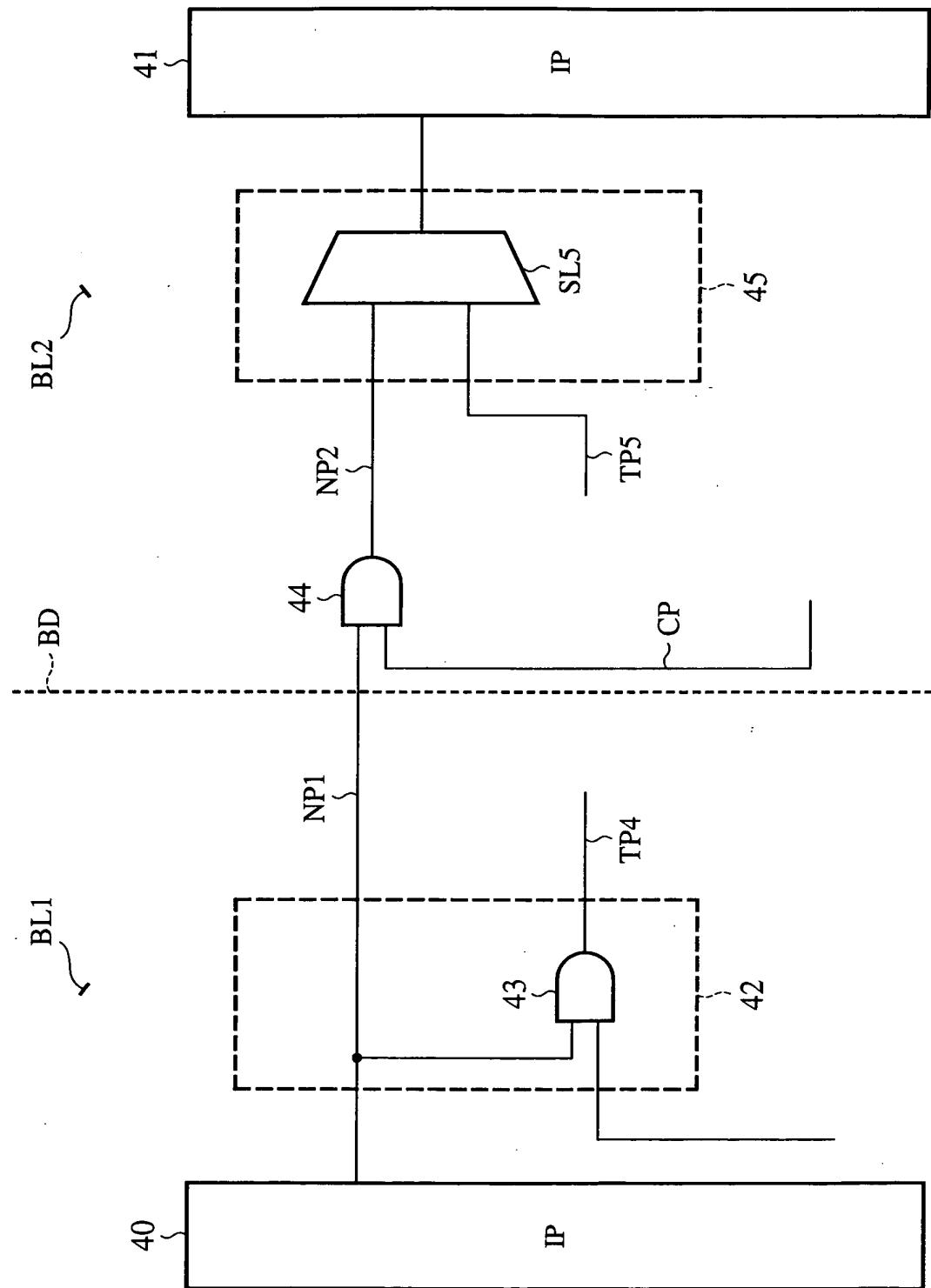


FIG.14

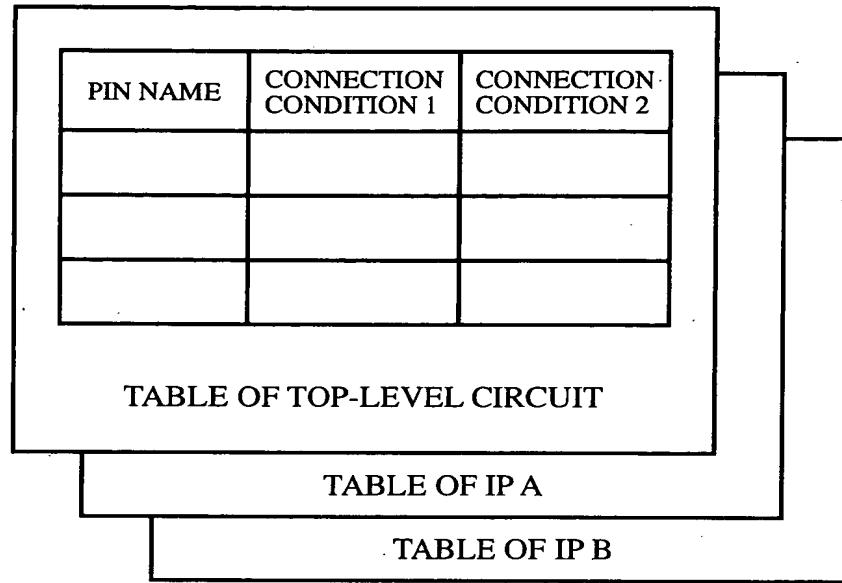
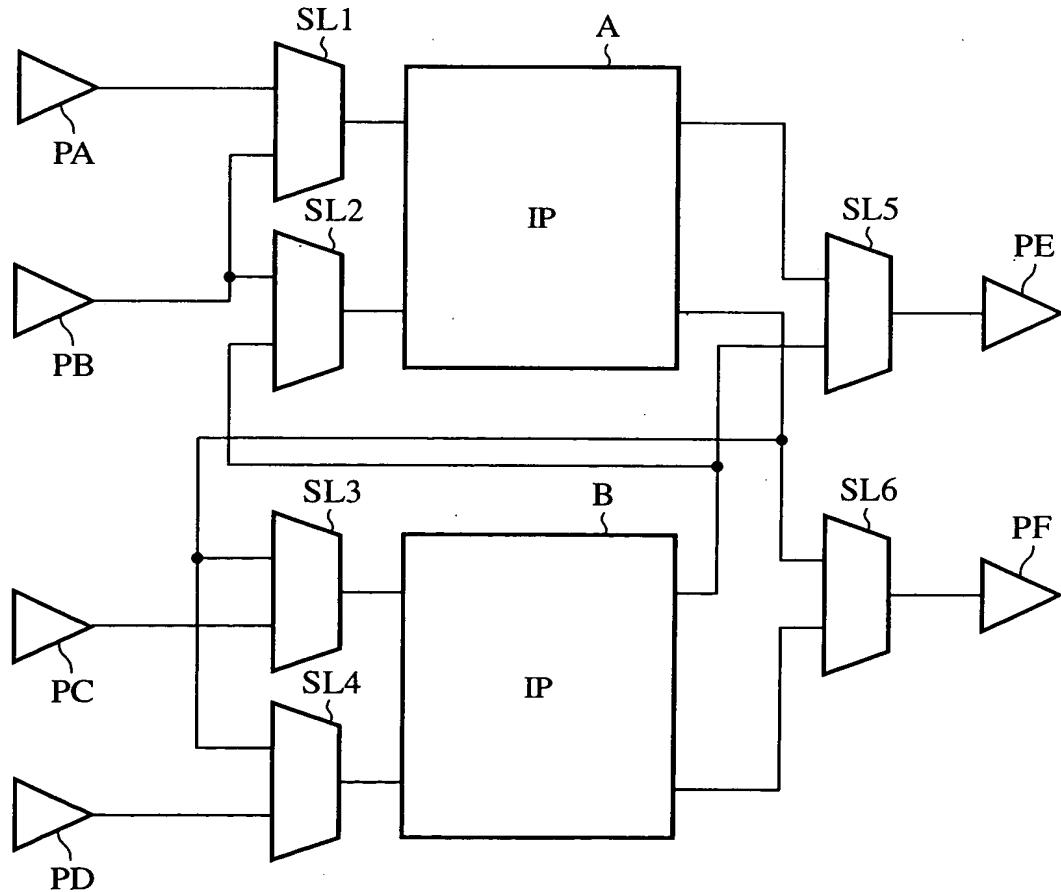


FIG.15



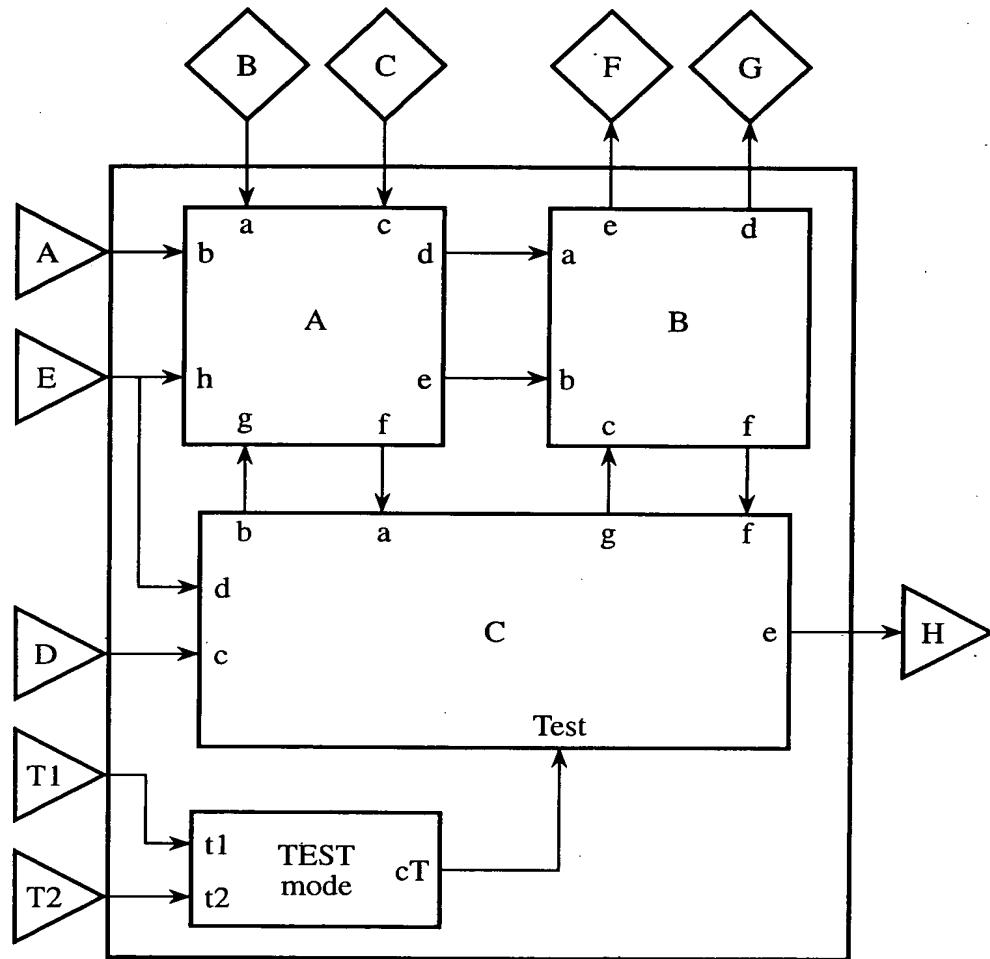
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FIG. 16

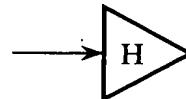
| POWER SUPPLY GROUP | A | ON |
|--------------------|---|----|
|--------------------|---|----|

| MODE SETTING PIN | NORMAL MODE SETTING |      |         | A CUTTING OUT MODE SETTING |    |      | B CUTTING OUT MODE SETTING |    |      | C CUTTING OUT MODE 1 SETTING |      |      | C CUTTING OUT MODE 2 SETTING |      |      |         |      |
|------------------|---------------------|------|---------|----------------------------|----|------|----------------------------|----|------|------------------------------|------|------|------------------------------|------|------|---------|------|
|                  | PIN                 | IO   | IP      | PIN(IP)                    | IO | IP   | PIN(IP)                    | IO | IP   | PIN(IP)                      | IO   | IP   | PIN(IP)                      | IO   | IP   | PIN(IP) | IO   |
|                  | A                   | Y    | Default | A                          | b  | I    | A                          | b  | I    | B                            | a    | I    | C                            | a    | I    | C       | a    |
| B                | A                   | L4   | -       | -                          | L  | -    | -                          | L  | -    | -                            | C    | b    | O                            | C    | b    | O       | C    |
| ↑                | Y                   | U200 | A       | a                          | I  | A    | a                          | I  | -    | -                            | -    | -    | -                            | -    | -    | -       | -    |
| ↑                | C                   | L    | H       | -                          | H  | -    | H                          | -  | H    | -                            | L    | -    | -                            | L    | -    | -       | -    |
| ↑                | IE                  | L    | H       | -                          | H  | -    | H                          | -  | H    | -                            | L    | -    | -                            | L    | -    | -       | -    |
| C                | A                   | H4   | L       | -                          | L  | -    | L                          | -  | L    | -                            | L    | -    | -                            | L    | -    | -       | -    |
| ↑                | Y                   | U200 | A       | c                          | I  | A    | c                          | I  | -    | -                            | MODE | subT | I                            | MODE | subT | I       | MODE |
| ↑                | C                   | L    | H       | -                          | H  | -    | H                          | -  | L    | -                            | -    | L    | -                            | -    | L    | -       | -    |
| ↑                | IE                  | L    | H       | -                          | H  | -    | H                          | -  | L    | -                            | -    | L    | -                            | -    | L    | -       | -    |
| D                | Y                   | L    | C       | c                          | I  | A    | g                          | I  | B    | c                            | I    | C    | c                            | I    | C    | c       | I    |
| E                | Y                   | L    | C       | d                          | I  | A    | h                          | I  | B    | b                            | I    | C    | d                            | I    | C    | d       | I    |
| ↑                | ↑                   | A    | h       | I                          | -  | -    | -                          | -  | -    | -                            | -    | -    | -                            | -    | -    | -       | -    |
| F                | A                   | L4   | B       | e                          | O  | A    | d                          | O  | B    | e                            | O    | C    | g                            | O    | C    | g       | O    |
| ↑                | Y                   | D200 | -       | -                          | -  | -    | -                          | -  | -    | -                            | -    | -    | -                            | -    | -    | -       | -    |
| ↑                | C                   | L    | A       | FCL                        | O  | L    | -                          | -  | L    | -                            | -    | L    | -                            | -    | L    | -       | -    |
| ↑                | IE                  | L    | A       | FCL                        | O  | L    | -                          | -  | L    | -                            | -    | L    | -                            | -    | L    | -       | -    |
| G                | A                   | H4   | B       | d                          | O  | A    | e                          | O  | B    | d                            | O    | L    | -                            | -    | L    | -       | -    |
| ↑                | Y                   | D200 | -       | -                          | -  | -    | -                          | -  | -    | -                            | -    | C    | f                            | I    | C    | f       | I    |
| ↑                | C                   | L    | L       | -                          | -  | L    | -                          | -  | L    | -                            | -    | H    | -                            | -    | H    | -       | -    |
| ↑                | IE                  | L    | L       | -                          | -  | L    | -                          | -  | L    | -                            | -    | H    | -                            | -    | H    | -       | -    |
| H                | A                   | L2   | C       | e                          | O  | A    | f                          | O  | B    | f                            | O    | C    | e                            | O    | C    | e       | O    |
| T1               | Y                   | L    | MODE    | t1                         | I  | MODE | t1                         | I  | MODE | t1                           | I    | MODE | t1                           | I    | MODE | t1      | I    |
| T2               | Y                   | L    | MODE    | t2                         | I  | MODE | t2                         | I  | MODE | t2                           | I    | MODE | t2                           | I    | MODE | t2      | I    |

FIG.17



BIDIRECTIONAL PIN



OUTPUT-ONLY PIN



INPUT-ONLY PIN

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FIG.18

| POWER SUPPLY GROUP | B | ON-OFF |
|--------------------|---|--------|
|--------------------|---|--------|

| MODE SETTING PIN | NORMAL MODE SETTING |         |     | A CUTTING OUT MODE SETTING |    |     | B CUTTING OUT MODE SETTING |    |    | C CUTTING OUT MODE 1 SETTING |    |    | C CUTTING OUT MODE 2 SETTING |    |    |
|------------------|---------------------|---------|-----|----------------------------|----|-----|----------------------------|----|----|------------------------------|----|----|------------------------------|----|----|
|                  | PAD                 | T1      | 0   | PAD                        | A  | 0   | PAD                        | B  | 1  | PAD                          | C  | 1  | PAD                          | D  | 1  |
| PAD              | T1                  | 0       |     | PAD                        | A  | 1   | PAD                        | A  | 1  | PAD                          | C  | 1  | PAD                          | D  | 1  |
| PAD              | T2                  |         |     | PAD                        | C  | 1   | PAD                        | C  | 1  | PAD                          | C  | 1  | PAD                          | D  | 1  |
| PAD              | C                   | -       |     | PAD                        | a  | O   | PAD                        | F  | O  | PAD                          | G  | O  | PAD                          | D  | -  |
| <b>BLOCK</b>     |                     |         |     |                            |    |     |                            |    |    |                              |    |    |                              |    |    |
| PIN              | IO                  | Default | IP  | PIN(IP)                    | IO | IP  | PIN(IP)                    | IO | IP | PIN(IP)                      | IO | IP | PIN(IP)                      | IO | IP |
| a                | I                   | L       | PAD | B                          | I  | PAD | B                          | I  | L  | -                            | -  | L  | -                            | -  | L  |
| b                | I                   | H       | PAD | A                          | I  | PAD | A                          | I  | L  | -                            | -  | L  | -                            | -  | L  |
| c                | I                   | L       | PAD | C                          | I  | PAD | C                          | I  | L  | -                            | -  | L  | -                            | -  | L  |
| d                | O                   | -       | B   | a                          | O  | PAD | F                          | O  | -  | -                            | -  | -  | -                            | -  | -  |
| e                | O                   | -       | B   | b                          | O  | PAD | G                          | O  | -  | -                            | -  | -  | -                            | -  | -  |
| f                | O                   | -       | C   | a                          | O  | PAD | H                          | O  | -  | -                            | -  | -  | -                            | -  | -  |
| g                | I                   | H       | C   | b                          | I  | PAD | D                          | I  | L  | -                            | -  | L  | -                            | -  | L  |
| FLC              | O                   | -       | PAD | F                          | O  | -   | -                          | -  | -  | -                            | -  | -  | -                            | -  | -  |
| h                | I                   | L       | PAD | E                          | I  | PAD | E                          | I  | L  | -                            | -  | L  | -                            | -  | L  |

FIG. 19

| POWER SUPPLY GROUP | B | ON-OFF |
|--------------------|---|--------|
|--------------------|---|--------|

| MODE SETTING PIN | NORMAL MODE SETTING |         |    | A CUTTING OUT MODE SETTING |         |    | B CUTTING OUT MODE SETTING |         |       | C CUTTING OUT MODE 1 SETTING |         |    | C CUTTING OUT MODE 2 SETTING |         |    |
|------------------|---------------------|---------|----|----------------------------|---------|----|----------------------------|---------|-------|------------------------------|---------|----|------------------------------|---------|----|
|                  | IP                  | PIN(IP) | IO | IP                         | PIN(IP) | IO | IP                         | PIN(IP) | IO    | IP                           | PIN(IP) | IO | IP                           | PIN(IP) | IO |
| PAD T1           | 0                   | -       | -  | 0                          | -       | -  | PAD F                      | 0       | -     | -                            | -       | -  | -                            | -       | -  |
| PAD T2           | 0                   | -       | -  | 1                          | -       | -  | PAD G                      | 0       | -     | -                            | -       | -  | -                            | -       | -  |
| PAD C            | -                   | -       | -  | -                          | -       | -  | PAD A                      | 1       | L     | -                            | -       | L  | -                            | -       | -  |
| BLOCK            |                     |         |    |                            |         |    | PAD E                      | 1       | L     | -                            | -       | L  | -                            | -       | -  |
| PIN              | IO                  | Default |    | IP                         | PIN(IP) | IO | IP                         | PIN(IP) | IO    | IP                           | PIN(IP) | IO | IP                           | PIN(IP) | IO |
| e                | O                   | -       |    | PAD F                      | O       | -  | -                          | -       | PAD F | 0                            | -       | -  | -                            | -       | -  |
| d                | O                   | -       |    | PAD G                      | O       | -  | -                          | -       | PAD G | O                            | -       | -  | -                            | -       | -  |
| a                | I                   | L       |    | A                          | d       | I  | L                          | -       | -     | PAD A                        | 1       | L  | -                            | -       | L  |
| b                | I                   | H       |    | A                          | e       | I  | L                          | -       | -     | PAD E                        | 1       | L  | -                            | -       | L  |
| c                | I                   | L       |    | C                          | g       | I  | -                          | -       | *     | PAD D                        | I       | -  | *                            | -       | *  |
| f                | O                   | -       |    | C                          | f       | O  | -                          | -       | -     | PAD H                        | O       | -  | -                            | -       | -  |

FIG.20

| POWER SUPPLY GROUP | A | ON |
|--------------------|---|----|
|--------------------|---|----|

| MODE SETTING PIN |    |         | A CUTTING OUT MODE SETTING |         |    | B CUTTING OUT MODE SETTING |         |    | C CUTTING OUT MODE 1 SETTING |         |     | C CUTTING OUT MODE 2 SETTING |         |     |      |      |   |
|------------------|----|---------|----------------------------|---------|----|----------------------------|---------|----|------------------------------|---------|-----|------------------------------|---------|-----|------|------|---|
| PIN              | IO | Default | IP                         | PIN(IP) | IO | IP                         | PIN(IP) | IO | IP                           | PIN(IP) | IO  | IP                           | PIN(IP) | IO  |      |      |   |
| d                | 1  | L       | PAD                        | E       | I  | L                          | -       | L  | -                            | PAD     | E   | I                            | PAD     | E   | I    |      |   |
| c                | 1  | H       | PAD                        | D       | I  | L                          | -       | L  | -                            | PAD     | D   | I                            | PAD     | D   | I    |      |   |
| e                | 0  | -       | PAD                        | H       | O  | -                          | -       | -  | -                            | PAD     | H   | O                            | PAD     | H   | O    |      |   |
| a                | 1  | L       | A                          | f       | I  | H                          | -       | -  | H                            | -       | -   | PAD                          | A       | I   | PAD  | A    | I |
| b                | 0  | -       | A                          | g       | O  | -                          | -       | -  | -                            | PAD     | B   | O                            | PAD     | B   | O    |      |   |
| f                | 1  | L       | B                          | f       | I  | -                          | *       | -  | -                            | *       | PAD | G                            | I       | PAD | G    | I    |   |
| g                | 0  | -       | B                          | c       | O  | -                          | -       | -  | -                            | -       | PAD | F                            | O       | PAD | F    | O    |   |
| test             | 1  | L       | MODE                       | cT      | I  | MODE                       | cT      | I  | MODE                         | cT      | I   | MODE                         | cT      | I   | MODE | cT   | I |
| PCA              | 0  | -       | MODE                       | AtoC    | O  | MODE                       | AtoC    | O  | MODE                         | AtoC    | O   | MODE                         | AtoC    | O   | MODE | AtoC | O |
| PCB              | 0  | -       | MODE                       | BtoC    | O  | MODE                       | BtoC    | O  | MODE                         | BtoC    | O   | MODE                         | BtoC    | O   | MODE | BtoC | O |